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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,776	09/30/2003	Jimmie Earl DeWitt JR.	AUS920030481US1	6262

35525 7590 12/18/2008

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ART UNIT	PAPER NUMBER
2193	

NOTIFICATION DATE	DELIVERY MODE
12/18/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/675,776	DEWITT ET AL.	
	Examiner	Art Unit	
	TUAN A. VU	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6,26,29,30,32,34,35,38 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 6, 26, 29-30, 32, 34-35, 38-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 9/23/08.

As indicated in Applicant's response, claims 1, 32, 39 have been amended, and claims 2, 27-28, 31, 33, 36-37, 40-48 canceled. Claims 1, 6, 26, 29-30, 32, 34-35, 38-39 are pending in the office action.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 6, 21, 25 of copending Application No. 10/675777 (hereinafter '777).

Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observations.

As per instant claims 1, 32, '777 claims 6, 21, 25 also recite determining for a instruction during execution for a association of an indicator associated with receiving a bundle or instruction in a instruction cache; associating a counter based on such determination and incrementing a counter in response to the indicator association with the instruction or event associated with the indicator. The event counting and instruction cache as recited by '777 are construed as obvious representation to a runtime indicator (leading to a counter increment, in which incrementing is count of number of instructions execution) and sending from the cached instruction for execution of the instant claims. Further, '777 does not recite 'spare bit' for indicator identifying whether the instruction is to be monitored, but based on the indicator received into a cache, a bit type implementation as a slot within an received instruction would have been a obvious feature, enabling a monitoring to receive the instruction and increment a counter based on '777 paradigm.

4. Claims 1, 32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2, 10, 20 of copending Application No. 10/675778 (hereinafter '778). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observations.

As per claims 1, 32, '778 claims 2, 10, 20 recite receiving a instruction with an indicator generated from a instruction cache, wherein upon determining that an indicator is associated with an instruction and a signal from the cache instruction, incrementing the counter each time the instructions is executed based on said cache signal. Even though '778 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, this limitation of instruction associated with indicator from cache would made the sending a obvious step within runtime based on instruction being cached in view of the above association and counting event.

Further, '778 does not recite 'spare bit' for indicator identifying whether the instruction is to be monitored, but based on the indicator received into a cache, a bit type implementation as a slot within an received instruction would have been a obvious feature, enabling a monitoring to receive the instruction and increment a counter based on '778 paradigm.

5. Claims 1, 32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3, 17 of copending Application No. 10/675872 (hereinafter '872).

As per instant claims 1, 32, '872 claims 3, 17 also recite instruction to be monitored and sent from cache instruction, determining whether an instruction in execution is related with an runtime range 'indicator'; and counting each event associated with the instruction if the instruction is associated with that range indicator. Even though '872 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, said limitation of instruction with associated indicator would made the instruction cache receiving and sending obvious steps within runtime based on instruction being cached in view of the above known concept, and the incrementing responsive to association of instruction with the indicator. Even

though '872 explicitly recites that the indicator is a location within contiguous range, this location-within- range limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented (in which incrementing in terms of count of number of instructions execution) in view of the above association determination. Further, '872 does not recite 'spare bit' for indicator identifying whether the instruction is to be monitored, but based on the indicator received into a cache, a bit type implementation as a slot within an received instruction would have been a obvious feature, enabling a monitoring to receive the instruction and increment a counter based on '872 paradigm

6. Claims 6, 34, are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 4, 12, 20 of copending Application No. 10/675721 (hereinafter '721).

As per instant claims 6, 34, 43, '721 claims 4, 12, 20 also recite determining for a instruction during execution for a association of a indicator, shadow memory (Note: even though '721 does not recite counter in shadow memory per se, a set of indicators being sent for monitoring would have made the counter as obviously in the shadow memory); incrementing a counter in response to the indicator association with the instruction, and responsive to which, executing while incrementing said executing. At the time the invention was made, expediting execution using instruction cache associated with profiling was known concept. Even though '721 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, said limitation of instruction with associated indicator would made the instruction cache receiving and sending obvious steps within runtime based on instruction being cached in view of the above known concept, and the incrementing responsive to association of instruction

with the indicator. The instruction in the *routine of interest* as recited by '721 is construed as obvious representation to a runtime instruction that requires some action (e.g. to monitor or to trace/modify leading to a counter increment in which incrementing is in terms of count of number of executions) of the instant claims. Further, '721 does not recite 'spare bit' for indicator identifying whether the instruction is to be monitored, but based on the indicator received into a cache, a bit type implementation as a slot within an received instruction would have been a obvious feature, enabling a monitoring to receive the instruction and increment a counter based on '721 paradigm

7. Claims 1, 32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 12, 23 of copending Application No. 10/682385 (hereinafter '385).

As per instant claims 1, 32, '385 claims 1, 12, 23 also recite executing instructions and detecting indicators that specify counting of events associated with the executing (Note: even though '385 recites data values in memory specifying counting event, a runtime event such as those memory indicators can be analogous to on runtime indicator of the instant claim); and counting each event associated with indicators. At the time the invention was made, expediting execution using instruction cache associated with profiling was known concept. Even though '385 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, said limitation of executing instructions associated with indicators would made the instruction cache reception and the sending obvious steps within runtime based on instruction being cached in view of the above known concept, and the incrementing responsive to association of instruction with the indicator. Even though '385 explicitly recites that counting

events associated with execution based on detection of value indicators, this limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented (in which incrementing is in terms of count of number of executions) in view of the above association determination. Further, '385 does not recite 'spare bit' for indicator identifying whether the instruction is to be monitored, but based on the indicator received into a cache, a bit type implementation as a slot within an received instruction would have been a obvious feature, enabling a monitoring to receive the instruction and increment a counter based on '385 paradigm

Specification: Objection

8. A preliminary examination of this application reveals that it includes terminology which is so different from that which is generally accepted in the art to which this invention pertains that a proper search of the prior art turns into a burden to the extent that, for one prosecuting the merits of the invention, assessing as to what the invention actually amounts to become a complicated matter without undue experimentation or outstretching of resources. For examples, see following:

(i) "Instruction cache 300 processes instructions for execution ... instruction cache 300 determines which instructions are associated with indicators … when instruction cache 300 determines that an instruction …is present" (Specifications: 1st para, 2nd para, pg 23). The actions termed as 'processes' and 'determines' (as underlined) used in a context where *instruction cache 300* is actually performing *processing* and *determining* is not a well-accepted terminology in the closest and related computer fields of using *instruction cache*. Cache is hardware storage means created as a specialized part from memory to store frequently used data,

not to process instructions; while cache controller would be a separate unit in communication with cache to effectuate some operations upon the data contained or received in cache. Without further hardware implementation in the Disclosure regarding how this cache is equipped with some processing and determining capability being integral thereto, the above language is deemed far-fetched and required correction.

(ii) '… signals for these instructions are sent by instruction cache 300 … cache 300, detects the indicators and sends signals to performance' (3rd para, pg. 23, 1st para pg. 24) amounts to an action performed by instruction cache 300. This action of sending taken by a cache cannot be construed as a terminology well-accepted by related arts. Code in execution can send data to other parts of the computer or network. A dedicated controller in communication to cache would reasonably be such hardware/software entity capable of *sending*, which is nowhere disclosed to support the above hard-to-accept terminology. In other words, no standard cache is well-known --without further teachings from the Specifications-- as being capable to actively send data.

(iii) 'the data and indicators are processed by a data cache, such as data cache 216 … data cache sends signals indicating that marked memory locations' (last para pg. 24). One familiar with the art of using or implementing cache cannot accept functionality of cache in terms being able to *process* data and actively *transmit* signals, absent clear teaching provided by the Disclosure to that regard.

Applicant is required to provide a clarification of these matters or correlation with art-accepted terminology so that a proper comparison with the prior art can be made. Applicant should be careful not to introduce any **new matter** into the disclosure (i.e., matter which is not supported by the disclosure as originally filed).

For the sake of prosecution, the above non-accepted terminology is construed as a mere **objection** to a language misuse and will be treated as though it is the host processor connected to cache (data or instruction cache 300) which is the entity or device supporting the functionality expressed by the above misuse of language (emphasis added).

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 1, 6, 26, 29-30, 32, 34-35, 38-39 are rejected under 35 U.S.C. 101 because the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility.

Claim 1 recites 'receiving a bundle at an instruction cache … determining by the instruction cache whether the bundle contains ... responsive to a determination … sending by the instruction cache ... sending the bundle from the instruction cache'. The actions leading to a result that a functional unit would execute instruction are based on active role of an instruction cache in terms of determining regarding bit inside received bundle and sending based on the determining. The Disclosure teaches a processor in connection with a host/pci bridge which includes a controller and cache memory (Specifications: Fig. 1 and pg. 12); however, there is no hardware/software implementation describing a specific utility with substantial details to assert/establish the fact that cache such as mentioned does contain a capability reminiscent of a processing unit capable of receiving, then *processing* the input data and/or *determining* what to do with it, and *sending* it to another part of the computer as claimed. The language regarding how the instruction cache operates (see (i), (ii) (iii) in Objection to the Specifications) amounts

to a far-fetched terminology without evidence of utility (e.g. specific and established programmatic or hardware means in place) to corroborate to the credibility of such terminology and feasibility of how *the instruction cache* can provide and achieve the operation of *determining*, processing or *sending*.

Lacking proper specific and substantial utility as set forth above, the above claimed scenario amounts to a non-statutory subject matter; and along with claim 1, claims 6, 26, 29-30 are rejected under 35 U.S.C. 101 because the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility.

Claim 32 recites 'responsive to receiving ... determining by the instruction cache ... responsive to a determination that the bundle contains ... sending a signal by the instruction cache to a performance monitor unit'; and thus, regarding asserted capability of the 'instruction cache', the above actions amount to an empty teaching devoid of specific and substantial utility so to realize the expected activity. Again, in light of the above analysis, the scenario of the so-recited subject matter cannot achieve any reasonable result, a requirement for a statutory practical Application.

Claims 32, 34-35, 38-39 are also rejected under 35 U.S.C. 101 because the claimed invention is not supported by either a *specific and substantial* asserted utility or a well established utility.

The lack of support will be treated as though the host processor connected to cache (data or instruction cache 300) is the actual entity or device supporting the functionality expressed by the above misuse of language; that is, the phrase 'by the instruction cache' is given no patentable weight for the sake of prosecuting the merits of the claims.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

12. Claims 1, 6, 26, 29-30, 32, 34-35, 38-39 are also rejected under 35 U.S.C. 112, first paragraph. Specifically, since the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility for the reasons set forth above, one skilled in the art clearly would not know how to use the claimed invention.

Claim 1 recites 'receiving a bundle at an instruction cache … *determining by the instruction cache* whether the bundle contains ... responsive to a determination … *sending by the instruction cache* ... sending the bundle from the instruction cache'.

Claim 32 recites 'responsive to receiving … determining *by the instruction cache* … responsive to a determination that the bundle contains ... sending a signal *by the instruction cache* to a performance monitor unit'.

According to the analysis of the Specifications and the observations made in the § 101 rejection, the instruction cache is nowhere taught by the Disclosure as equipped with programmatic or hardware functionality in terms of executed actions of *processing*, *determining* then *sending*.

Claims 1, 6, 26, 29-30, 32, 34-35, 38-39 are rejected for belonging to a claimed invention not supported by either a specific and substantial asserted utility or a well established utility as set forth above.

The lack of utility deficiency will be treated as though the host processor connected to cache (data or instruction cache), is the actual entity or device supporting the functionality expressed by the above misuse of language; that is, the phrase 'by the instruction cache' is given no patentable weight for the sake of prosecuting the merits of the claims.

13. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. Claims 32, 36, 38-39 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the relationship between

determining by the instruction cache, sending by the instruction cache;

AND

code for receiving at an instruction cache, code for sending by the instruction cache, code for sending the bundle from the instruction cache (claim 32), *code for receiving a second bundle at the instruction cache, for determining whether the second bundle contains* (claim 39).

Claim 32 recites a computer medium to store code, the code for receiving at the instruction cache. One of ordinary skill would not be able to construe how *receiving at* a cache (a) is effectuated by a external medium containing code, nor can one understand (external) code when executed effectuates 'determining by the instruction cache' (b) or 'sending a bundle by a cache'(c) . As for (a), normal code in execution from a memory either sends data to a cache, or code inside a cache-based processor receives data for storing in that cache (emphasis added).

The functionality recited as 'code for receiving at a cache' appears a hard to construe functionality. The cache, as set forth in the USC 112, 1st paragraph, is not taught as having intrinsic code (for executing) as to receive data when the executing code as claimed in claim 32 resides in a separate storage medium. As for (b) and (c), code when executed would determine and send data somewhere outside from where data first resides; but code executed outside of cache to do 'determining by a cache' and 'sending by a cache' would not be plausible.

Likewise, as in **claim 39**, this same medium-stored code when executed effectuates 'receiving a second bundle at the instruction cache' (d), i.e. the concept of an external code providing a 'receiving' act become hard to construe. The **Specifications does not provide** a single passage describing **a medium containing executable code**, which when run, would effectuate (a) 'receiving *at* an instruction cache' of any bundle, or (b) or (c) or (d). There is omission of programmatic or structural elements between how cache receives bundle and how an external code executes 'receiving' at the cache; and how code executes 'sending a bundle by a cache'.

Moreover, the language of 'determining by the instruction cache' and 'sending by the instruction cache' (re claim 32) entail that code resides inside a cache to effectuate 'determining' and 'sending'. However, such functionality is found to have no utility or enabling support/means. The Specifications does not describe that a computer readable medium (distinct from a cache) is such that it will execute 'receiving at a cache', 'determining by a cache', and 'sending by a cache'. That is, there is an omission of essential teaching. One cannot construe a external code for determining and sending by the cache when the code for such resides in the computer readable medium that has nothing in common with the recited 'instruction cache'. The lack of

functionality of the cache (in terms of established utility) and the lack of relationship between determining and sending by cache and determining and sending by the computer medium code would not enable one to make use of the invention.

Claims 32, 36, 38-39 are rejected for indefinite language, in terms of omission of structural element relationship in order to help make use of the invention.

The receiving, determining, sending, would be treated as being effectuated by a host processor processing instructions or data in communication with cache and monitoring unit.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1, 6, 26, 29-30, 32, 34-35, 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gover et al., USPN: 5,752,062(hereinafter Gover) in view of APA (Admitted Prior Art: Specifications: Description of Related Art, pg. 2-3).

As per claim 1, Gover discloses a method in an instruction cache of a data processing system for monitoring execution of instructions, the method comprising:

receiving a bundle at an instruction cache, the bundle containing at least one instruction slot, wherein the instruction slot contains an instruction (e.g. Fig. 1; Fig. 3 – Note: instruction cache reads on slot containing an instruction);

determining *by the instruction cache* (Note: by the instruction cache treated as processor code – refer to USC 112, 1st rejection) whether the bundle contains an indicator (col. 7, lines 15

to col. 8, lines 17; Fig. 3) within at least one spare bit of the at least one instruction slot (Bit 17, Bit 18 – Fig 6A – Note: bit reserved for storing a indicating status reads on bit being spared for that purpose), wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit (*bit ... selected for counting* - col. 8, line 41 to col. 9, line 29);

responsive to a determination that the bundle contains the indicator within the at least one instruction slot, sending a signal (interrupt - col. 9, lines 30 to col. 10, line 5; Fig. 7) *by the instruction cache* (see USC 112 1st Rejection) to a performance monitor unit,

wherein upon receiving the signal, the performance monitor unit increments (col. 11 lines 4-37) a counter associated with the instruction wherein the incrementing provides a count of a number of times the instruction is executed (allowing counting, counting enablement – col. 11 lines 25-35; Fig. 6A); and

sending the bundle from the instruction cache to a functional unit for execution of the instruction (e.g. Fig. 2).

Gover does not explicitly disclose that determining that indicator in the received bundle identifies instruction to be monitored *is responsive to receiving the bundle at the instruction cache*. Gover discloses sequencer unit using special registers to store information received from instructions received from cache (col. 5 lines 5-30) for a reordering processes based on condition fields stored in those reorder buffers, the information including 'completion' 'finished' and 'exception field' (col. 6 line 53 to col. 7 line 33; col. 7 line 62 to col. 8 line 17) and based on which dispatch the instruction to other executing units accordingly. Based on the special registers being used to have field/bit indicating an exception whereby the monitoring unit operates in synchronization within a multiprocessor environment (time base facility ... interrupt -

col 8 line 46 to col 9 line 46), the necessary act of interpreting a state indicator such as 'completed' similar to those used by the dispatch unit (completion 80, exception 82 - Fig 2) with respect to a loaded instruction (col. 10 lines 57-63) in conjunction with the monitoring unit responding to an 'exception' bit or field in the MMCRx (see Fig. 6A; col. 11 lines 4-37) is indicative that responsive to a loaded instruction from cache; that is, the dispatching unit thereby coordinates with special registers and interprets some exception information therein to coordinate action for a performance monitoring unit. Based on the use of special register, it would have been obvious for one skill in the art at the time the invention was made to implement Gover's reordering process via a scheduler or dispatching unit (see Fig. 2) so that in response to a bundle received from instruction cache, whereby a indicator information related to an instruction therein is interpreted as indication a state to address (e.g. completed, finished, exception), the scheduling process dispatches the indicated instruction (i.e. handling a exception field as indicated by a register bit) to the monitoring unit as taught above (col. 11 lines 4-37) because this would enable the performance monitoring unit to be synchronized functionally with the rest of the process in Gover's multiprocessing system (see col. 19 line 28 to col. 20 line 30)

As per claim 6, Gover discloses wherein the counter is located in a shadow memory (col. 8, lines 26-39 – Note: special registers and PMCs with state or content – MMCRn -- maintained via special privilege access mode and being kept in parallel with execution scheduling – see col. 11, lines 14-50 -- as informational support thereof, hence reads on shadowing type of information kept in memory; see SSR col. 9 lines 36-57).

As per claim 26, Gover does not explicitly disclose comprising using a spare field in the bundle to contain the indicator; but based on the indicators received by the execution unit sent by

the sequencer and based on which to execute some needed performance monitoring action (see Fig. 6a-b), it would have been obvious for one skill in the art at the time the invention was made to enable a special field in the bundle as set forth in claim 1 so that a spare slot contains this indicator, among the other slots that are primarily allotted for the instruction per se (see Fig. 3).

As per claim 29, Gover discloses responsive to a determination that the bundle contains the indicator, beginning incrementing the counter, wherein the counter (refer to claim 27-28) tracks any subsequent instruction executed by an associated processor (e.g. *to correspond to a particular processor* – col. 8, lines 46-55).

As per claim 30, Gover does not disclose receiving a second bundle at the instruction cache; responsive to receiving the second bundle, determining whether the second bundle contains a second indicator; and responsive to a determination that the second bundle contains the second indicator, ending incrementing the counter. But the scenario for receiving, determining responsive to an indicator, and sending signal to a performance monitoring unit has been addressed in claim 1 to enable proper synchronization of scheduled instructions. Based on the fetching of instruction from cache for a dispatching unit to store information in special registers (GPR, FPRs col 5 lines 6 to col 6 line 6) and how this stored information or bit/field indicators are used to support scheduling and Performance monitoring unit (Fig. 6A)as in a synchronization endeavored by Gover (see claim 1), it would have been obvious for one skill in the art at the time the invention was made to implement this receiving, determining of a monitoring indication, and sending signal for the performance monitoring unit so that a second instruction being fetched from the same cache, would be interpreted via indicator implemented thereby in order to support signal sending to the performance monitory unit exactly as this has

been implemented for the first instruction from the cache bundle as set forth in claim 1, because this would enable thorough Gover' s multi-processor system synchronization of all fetched instructions from cache as explained in the rationale of claim 1.

As per claim 32, Gover discloses a computer program product comprising:

a computer readable medium having computer usable program code for monitoring execution of instructions, the computer program product comprising computer usable program code for:

receiving a bundle at an instruction cache, the bundle containing at least one instruction slot, wherein the instruction slot contains an instruction;

determining *by the instruction cache* (see USC 112, 1st para) whether the bundle contains an indicator within at least one spare bit of the at least one instruction slot, wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit;

responsive to a determination that the bundle contains the indicator within the at least one instruction slot, sending a signal *by the instruction cache* (refer to USC 112 1st para) to a performance monitor unit,

wherein upon receiving the signal, the performance monitor unit increments incrementing a counter associated with the instruction wherein the incrementing provides a count of a number of times the instruction is executed; and

sending the bundle from the instruction cache to a functional unit for execution of the instruction;

all of which having been addressed in claim 1.

Gover does not explicitly disclose that determining that indicator in the received bundle identifies instruction to be monitored *is responsive to receiving the bundle at the instruction cache*. However, this limitation has been obvious as set forth in the rationale of claim 1.

As per claim 34, refer to claim 6.

As per claims 35, 38, 39 refer to claims 26, 29, 30 respectively..

Response to Arguments

17. Applicant's arguments filed 9/23/08 have been fully considered but they are not persuasive. Following are the Examiner's observation in regard thereto.

35 USC § 103 Rejection:

(A) Applicants have submitted that Gover does not disclose 'determining by the instruction cache … indicator within … one spare bit … instruction slot' (Appl. Rmrks pg. 10 bottom). The newly changed claim limitation has been met with new grounds of rejection. Because the rejection has been necessitated by the Amendments, the argument for alluding to changed subject matter would be deemed largely moot.

(B) Applicants have submitted that none of the cited portions in Gover to reject the unamended claims (Appl. Rmrks pg. 11 middle) discloses 'determining by the instruction cache … spare bit … instruction slot' (Appl. Rmrks pg. 12 top 2 para). The argument is referred back to section A in view of the amendment to the current claimed subject matter.

(C) Applicants have submitted for claims 6, 26, 29-30, 32, 34-35, 38-39, there is nothing in Gover discloses 'determining by the instruction cache … instruction slot'. The argument is not deemed sufficient to overcome the current state of the Rejection.

Response to Examiner's Assertions:

(D) Applicants have submitted that Applicant is not claiming instructions being sent to the performance monitor (Appl. Rmrks pg. 14, top) rendering Examiner's Assertion erroneous. The argument is not pointing how a particular language of the claim is not matched by the Office Action citing of Gover, especially when 'sending a signal' is a limitation being part of the Amendment being addressed by the current Office Action. The argument is deemed moot or misplaced.

(E) Applicants have submitted that Examiner's adopting of an 'ultra-narrow' view of 'cache' for storage purpose only, when 'cache' should be understood as to also include a 'cache controller' (Appl. Rmrks pg. 14, middle). Assertion by the Applicants *without explicit and deliberate definition* of cache anywhere in the Disclosure so as to unequivocally establish that *cache* as utilized in the invention will include a controller with processing functionality therein would be deemed mere assertion having no probative impact. For one of ordinary skill in the art if cache is to be understood as inherently having a processor therein, such feature would appear too particular to be accepted by any standard regarding a definition of a cache. Cache is a static storage part, whereas a controller is a active part/device. For example, a 'cache controller' including processor capability and in physical communication with a 'cache' can process instruction stream; and such scenario has to be explicit disclosed and in place for one to give weight. Therefore, the literal term 'instruction cache' used in the Disclosure without explicit attachment to any other controller can only signify a static storage means. Lack of support by the Disclosure as a whole as to establish that 'cache' does have processing functionality (i.e. including a processor therein capable of receiving, processing, determining and sending signal) has been deemed a statutory type deficiency, as set forth in the Office Action. Mere pleading by

Applicants without providing factual evidence is deemed not persuasive to overcome the above lack of support rejection.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (571) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571)272-3759.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence - please consult Examiner before using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Tuan A Vu/

Primary Examiner, Art Unit 2193

December 14, 2008